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TRANSISTORIZED VHF TRANSMITTER DESIGN FOR SPACECRAFT APPLICATIONS

by Charles R. Somerlock

*Goddard Space Flight Center
Greenbelt, Maryland*

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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SUMMARY

Little has been published about VHF transmitter design employing transistors. Because of the fact that these devices are operating so far down on the frequency response curve, detailed circuit analysis is very difficult. However, with the use of liberal approximations and some experimental results, a rough design can be made. A design of a satellite transmitter is made as an example of the procedure. Such a transmitter demonstrates advanced practice in the use of radio frequency transistors as well as an application, which is itself of interest. As verification of the method, the sample transmitter was built and tested.

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INTRODUCTION

In this age of transistor electronics, when solid state circuitry is replacing the more familiar vacuum tubes in many fields, there appears to be a great lack of informative literature about VHF transmitter design employing transistors. Of special interest is the application to missile and space vehicle telemetry, since the requirements of light weight, low power drain, and rugged environmental capability make these devices ideal for this purpose.

This paper, therefore, presents a sample design for a VHF telemetry transmitter using transistors throughout. Various problems and pitfalls peculiar to the use of transistors and to this application are discussed, and suggestions are made to assist the inexperienced designer.

PHILOSOPHY OF CIRCUIT DESIGN

Oscillators

At the heart of every transmitter is an oscillator that generates the RF energy. Because of the frequency stability requirements of most transmitters, this oscillator is usually crystal-controlled. Use of a quartz crystal for frequency control does not necessarily guarantee good stability, however. Where the transmitter parameters can affect the frequency of oscillation, the frequency stability of the oscillator with temperature may be several times worse than that of the crystal itself. This is because the transistor parameters themselves are very temperature-sensitive. Accordingly, the transmitter oscillator circuit should be designed so that the frequency of oscillation is dependent solely on the quartz crystal. To help reduce the effect of the transistor, a transistor should be chosen with the highest possible cutoff frequency, so that its phase shift at the operating frequency is negligible.

For similar reasons, and to prevent the possibility of incidental frequency modulation from occurring, the oscillator frequency-determining elements should be isolated as well as possible

*Originally submitted to the University of Maryland as partial fulfillment of the requirements for the degree of Master of Science, 1963, under the title "A Transistorized VHF Transmitter."

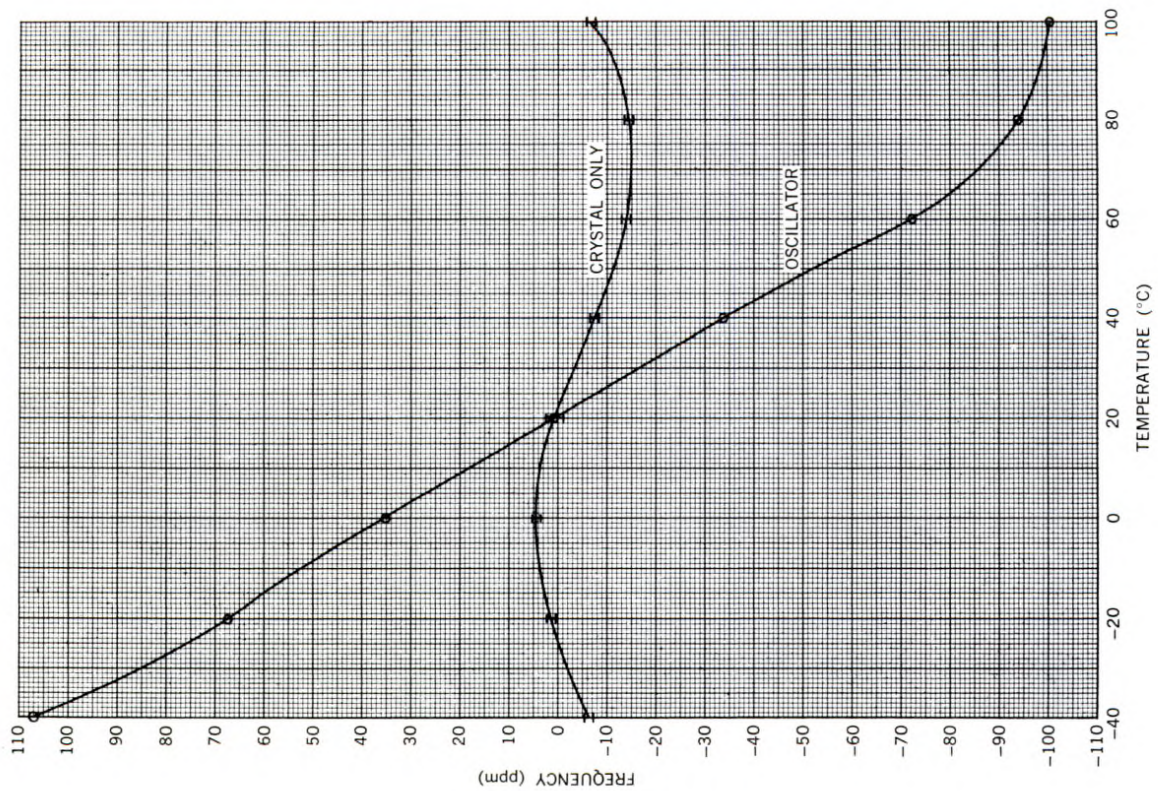


Figure 1—Frequency drift of a 17 Mc series mode oscillator [see Figure 4(a)].

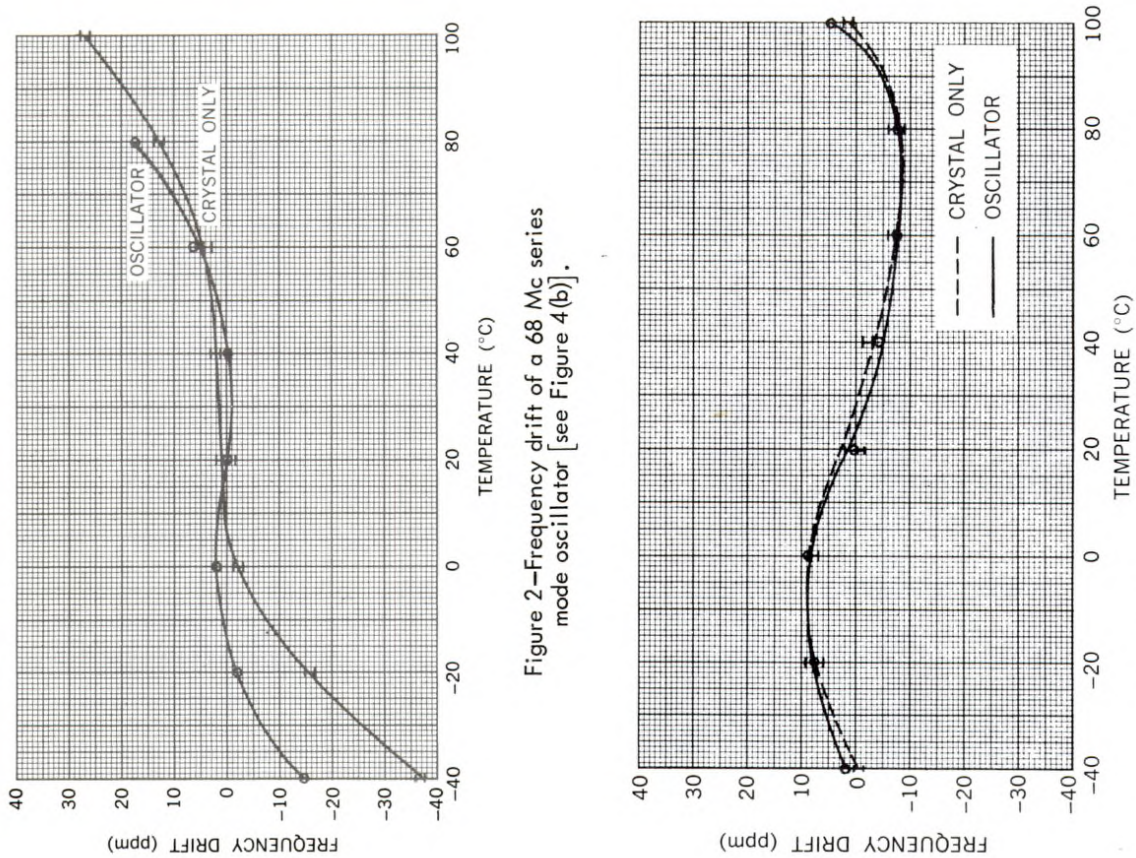


Figure 2—Frequency drift of a 68 Mc series mode oscillator [see Figure 4(b)].

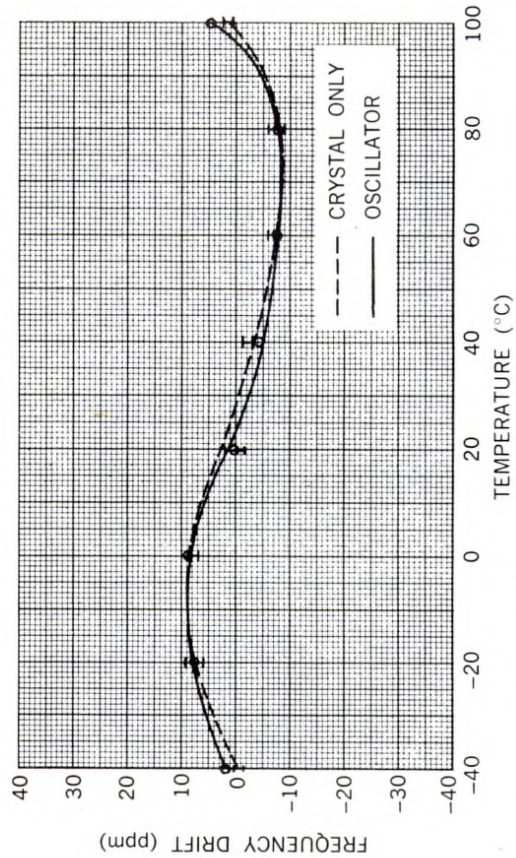


Figure 3—Frequency drift of a 17 Mc modified Pierce oscillator [see Figure 4(c)].

from the load impedance. The impedance of the load on the oscillator is sure to vary over the modulation cycle and over the temperature range, so care must be taken that it does not affect the oscillator frequency. When a phase-lock receiving system of narrow bandwidth is used, incidental frequency shifts of only a few cycles can cause distortion and difficulty in maintaining lock.

Figures 1, 2, and 3 compare the frequency versus temperature curves of certain oscillators to those of their quartz crystals alone. It is clear that the oscillator circuit used in Figures 1 and 2 allows elements other than the crystal to affect the frequency. This circuit, a series mode type that is widely used in VHF devices, is shown in Figures 4(a) and 4(b).

On the other hand, examine the circuit plotted in Figure 3, a modification of the familiar Pierce oscillator [see Figure 4(c)]. Within the limits of measurement error, its frequency is independent of all circuit elements except the crystal. This excellent characteristic is due partly to the fact that the crystal is the only resonant element in the whole oscillator and partly to the negative feedback that stabilizes the gain of the transistor. Also, since the oscillator is basically a Colpitts configuration, it retains all the advantages of that well-known circuit.

In a similar way, Figure 5 shows the effect that changes in load impedance have on these same oscillators. Again, the Pierce configuration shows excellent independence of loading while the series mode oscillator shows up poorly in comparison. The excellent stability of this oscillator under load is due to the large negative feedback provided by the emitter resistor. This feedback has the effect of lowering the output impedance of the circuit, making it insensitive to all but extremely low values of load resistance. The modified Pierce oscillator, while not the only type of oscillator that is usable, demonstrates the sort of performance that is recommended.

Along with good frequency stability, some degree of amplitude stability is usually required; but, as long as the output of the oscillator does not vary more than about 2 db, no problems will generally occur. This condition usually is easily met with class C oscillators, since their output amplitude is set by some limiting action in the circuit and plenty of excess gain is available to sustain oscillations.

Amplifiers

The high efficiency requirement of a transmitter amplifier stage dictates the use of class C operation in all but the lowest level stages. Class C circuits can be self-biased by placing a resistor in the dc path to ground from either the base or the emitter, where the signal current flowing will develop a reverse bias. Typical bias levels are usually less than 1 volt.

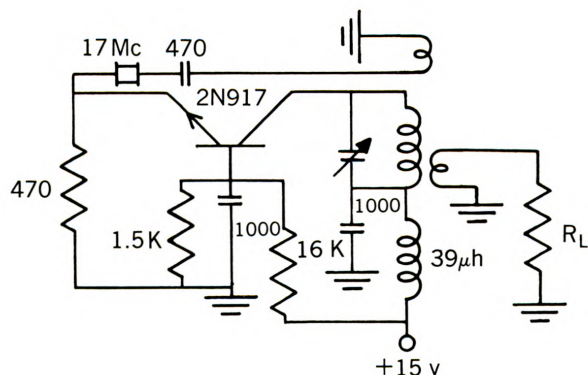
Because of the relatively low corner frequency of the gain versus frequency curve, the gain of even the best VHF power transistors available is only 6 to 10 db at 150 Mc. Typical collector efficiencies obtainable at this frequency are approximately 40 to 60 percent, including tank circuit efficiency. Calculating the expected power gain from the transistor collector curves as is done with vacuum tubes is an impossible task, since the operating point is so far down on the frequency response curve. Conventional small signal analysis is not adequate, since transmitter amplifier stages are

large signal devices. Performance parameters, measured at the frequency of interest and supplied by the manufacturer, must be used along with liberal approximations and – many times – experimental results. An additional complication is the wide variation of the transistor parameters allowed between

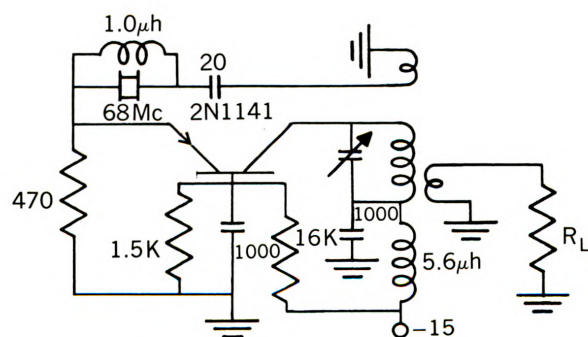
units of the same type by current practice in transistor manufacture. Because of these difficulties, detailed time-consuming analysis of transistor class C power amplifiers is not profitable. The liberal use of approximations and assumptions based on experience and experiment is justified and will yield results that are just as reliable as the more detailed ones based on invalid processes.

The design of an amplifier stage begins with the choice of the supply voltage for the transistor to be used. For maximum efficiency and gain, the supply voltage should be as high as practicable without exceeding the collector breakdown voltage of the transistor. Since the peak-to-peak signal voltage is approximately twice the supply voltage, the supply is limited to:

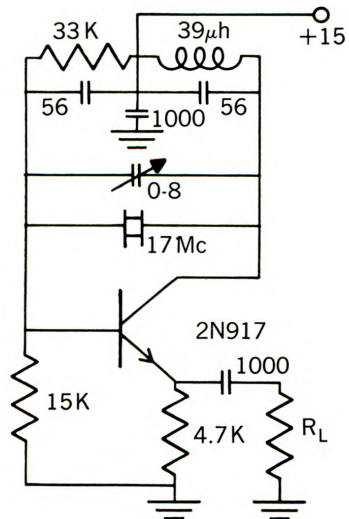
$$V_{cc} \approx \frac{1}{2} V_{ce}, \text{ or } \frac{1}{2} V_{cb},$$



(a) 17Mc series resonant oscillator



(b) 68Mc series resonant oscillator



(c) 17Mc modified Pierce oscillator

Figure 4—Oscillator circuits.

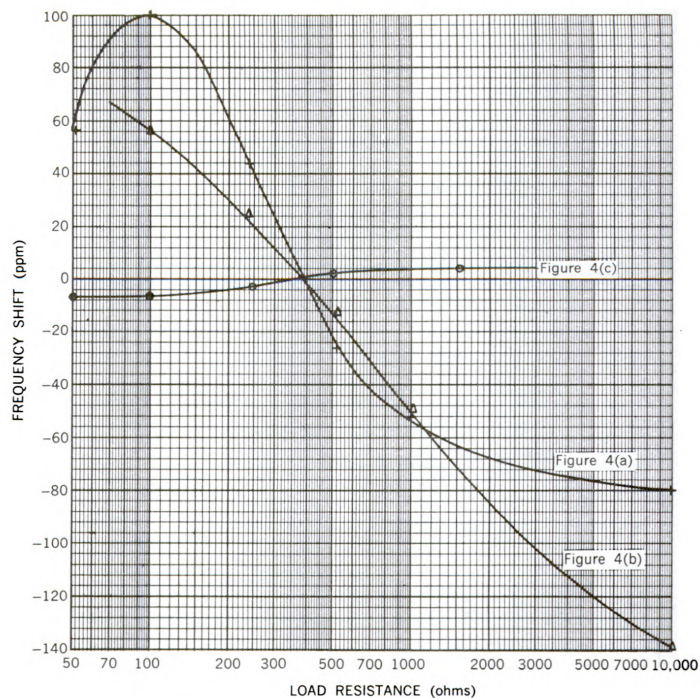


Figure 5—Effect of oscillator load resistance.

depending on the configuration. (All symbols are defined in Appendix A.) The grounded base circuit has demonstrated greater stability than the grounded emitter type and has only a negligibly smaller power gain.

Once the voltage and the required output power are known, the plate load resistance can be found:

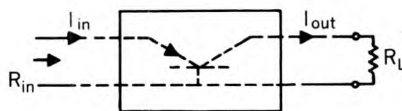
$$R_L = \frac{V_c^2}{2P_o} \approx \frac{V_{cc}^2}{2P_o} ,$$

from which the tank circuit parameters follow:

$$X_C = X_L = \frac{R_L}{Q} .$$

Optimum Q for a class C amplifier is typically 10 to 20, representing a balance between selectivity and tank circuit efficiency.

A relation between input resistance and power gain can be developed as follows:



$$I_{in} = \frac{I_{out}}{G_i} ,$$

$$P_{in} = \frac{P_o}{G_p} ,$$

$$R_{in} = \frac{P_{in}}{(I_{in})^2} = \frac{P_o/G_p}{I_{out}^2/G_i^2} = R_L \frac{G_i^2}{G_p} ;$$

for grounded base and $f \ll f_{max}$:

$$G_i \approx 1 ,$$

$$R_{in} \approx \frac{R_L}{G_p} .$$

Usually, measured curves of power gain versus frequency are available from the transistor data sheets. Where these are not available, the process must be reversed to find G_p from R_{in} , which to a first approximation can be assumed to be $1/\text{Re}Y_{ib}$. The latter approximation is generally not too good, however.

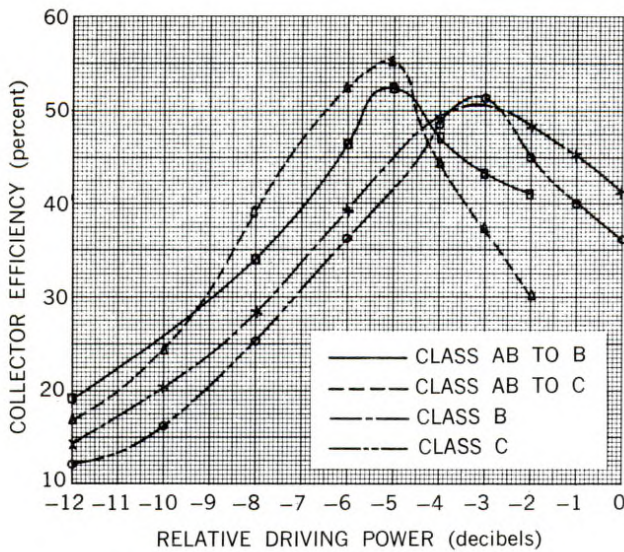


Figure 6—Amplifier collector efficiency.

Any of the usual methods of interstage coupling that will match the impedances can be used. Capacitive coupling methods seem to work out better, though — probably because they can be adjusted more readily to optimum conditions. One simple coupling method is connecting the stages with a small value capacitor. The collector load impedance is then simply the parallel equivalent of the series combination of the coupling capacitor and the input resistance of the next stage. Assuming R_L/R_{in} is greater than about 25,

$$R_L = Q^2 R_{in} = \left(\frac{X_c}{R_{in}} \right)^2 R_{in} = \frac{X_c^2}{R_{in}} ;$$

so

$$X_c = \sqrt{R_L R_{in}} .$$

The equivalent parallel capacitance (approximately X_c) will, of course, have to be counted as part of the tank circuit capacity.

A major problem with transistor amplifiers is gain stability. The gain of such a device will vary over the temperature range. For this reason, it is desirable to operate the amplifier in a slightly saturated condition. Figure 6 shows how this type of operation will sacrifice some efficiency, but it is necessary if the output power is to be independent of the ambient temperature. For the same reason, the response of the amplifier below the saturated state should be nearly linear. As seen in Figure 7 the class C amplifier is not linear, small changes in drive causing larger changes in output. Thus in a transmitter employing several class C stages, a small drop in oscillator output can be greatly magnified.

The response can be made more linear (Figure 7) if a small forward bias is applied to the base as shown in Figure 8. At normal output, the self-generated reverse bias overcomes the fixed forward bias, and the operation is class C. As the drive level drops, however, the bias tends more toward

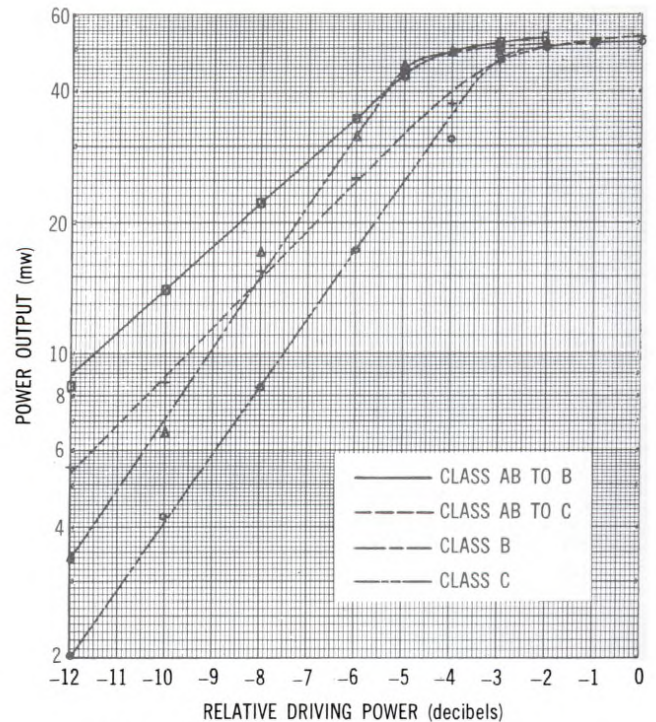


Figure 7—Amplifier drive characteristics.

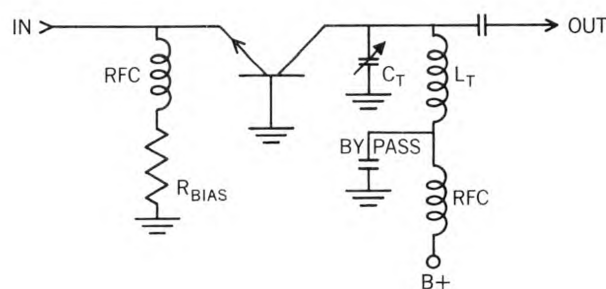
forward bias, the gain increases, and a nearly linear output results. Even better regulation can be obtained if the forward bias is developed across an external diode placed in series with the base. The diode will then compensate for the change in the base-emitter voltage drop with temperature variations.

Feedback, both internal and external to the transistor, is also frequently a problem. It usually manifests itself as either outright regeneration or as a "hysteresis" effect in the amplifier tuning characteristic. In theory, unilateralization is the obvious answer. In practice, though, unilateralization of large signal transistor VHF amplifiers is difficult. Because the transistor is operating near its cutoff frequency, it has a large phase shift. This phase shift requires use of somewhat more complex feedback networks, the components of which must be determined practically by trial and error. With a few precautions, however, the difficult unilateralization problem can be bypassed.

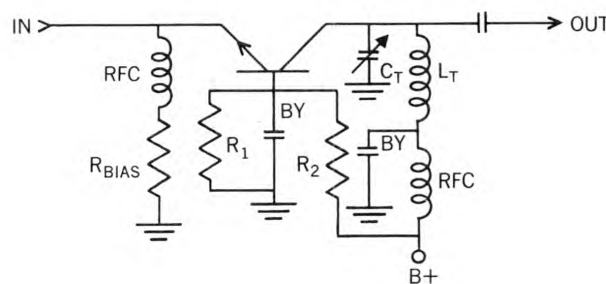
Care should be taken to eliminate all sources of feedback external to the transistor. Among common sources are inadequate shielding, excessive lead lengths (particularly the "common" transistor lead), and chassis currents. The latter two failings are frequently overlooked by novice designers. For good shielding, the "egg crate" style of packaging is recommended. Good grounding of the "common" transistor lead can be accomplished where physical conditions limit the shortness of the lead by series-tuning of the lead inductance with a bypass capacitor slightly smaller than normal. Caution is important here, so that the bypassing is not underdone. Chassis currents are frequent sources of feedback in transmitters where large power gains are present. One example of this problem is the grounding of a transistor lead in the current path between a tank inductor bypass and the tank capacitor mounting. There is a large circulating current in this path that, in a careless effort to increase packaging density, can cause real problems.

The grounded base circuit is highly recommended over the grounded emitter for stability. While the common base circuit has only slightly less power gain at VHF frequencies and large signal conditions than the common emitter circuit, it demonstrates a much smaller internal feedback problem.

The choice of the proper transistor can be important to this problem also: generally, the higher the transistor's cutoff frequency, the lower its inherent feedback. Accordingly, where several transistors are available, the one with the highest frequency rating should be chosen. With all other things equal, this will usually turn out to be the one that is most efficient and demonstrates the best gain.



CLASS C RF AMPLIFIER



CLASS C RF AMPLIFIER WITH FORWARD BIAS AT LOW SIGNAL LEVELS

Figure 8—Radio frequency amplifiers.

Buffer Amplifiers

Because of their internal feedback, transistors generally do not make very good buffer amplifiers. Neutralization will help, of course; but this is tricky, as was pointed out in the section on amplifiers. Figure 9 shows the effect of load resistance on the input resistance of an amplifier (Figure 10) in two classes of operation. The graph shows that the variation of input resistance becomes more severe after the amplifier saturates. For good buffer action, then, an amplifier should be loaded somewhat heavily so that it will not operate in a saturated condition. The class C mode of operation demonstrates a slight improvement in isolation over the class AB, but the superiority is slight. The extra gain of class A or AB operation may allow use of resistive padding for additional isolation with no increase in power requirements. An emitter follower or some other circuit employing negative feedback can be used where good isolation is important. These circuits however, have very low power gain, and overall efficiency will suffer somewhat. Emitter followers are also a little temperamental at VHF, sometimes developing parasitic oscillations under capacitive loads.

Frequency Multipliers

Since transistors are very nonlinear devices in large signal operation, they can be used effectively as frequency multipliers. The use of large reverse bias will enhance the efficiency and power gain in this type of operation because the harmonic distortion of the output current waveform is increased by the shorter conduction angle. Collector tank circuits with higher Q also should be used, so that effective rejection of the fundamental driving frequency is accomplished. Because of the fact that the available power gain at VHF for large signal amplifiers is already low, the gain of a frequency multiplier will be only 3 or 4 db usually; and it will decrease as the conduction angle is shortened. A compromise therefore must usually be made between efficiency of the stage and power gain (which will affect the overall system efficiency). At lower frequencies, performance, of course, increases. In a practical sense, however, multiplication greater than tripling in a single stage is too inefficient to be useful in a transmitter. Multiplier strings should, if possible, be arranged so that the desired order of frequency multiplication can be accomplished with cascaded doublers and triplers.

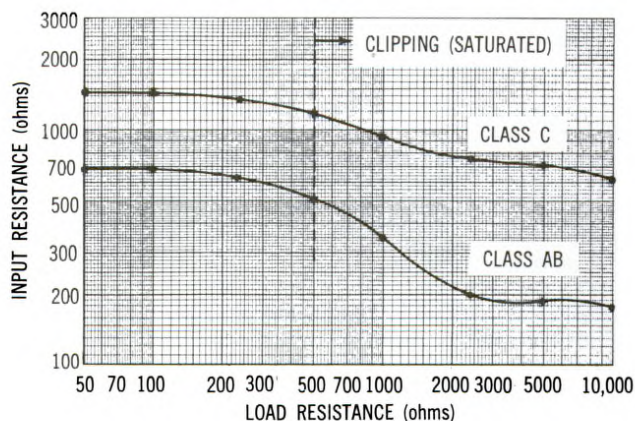


Figure 9—Effect of amplifier load resistance.

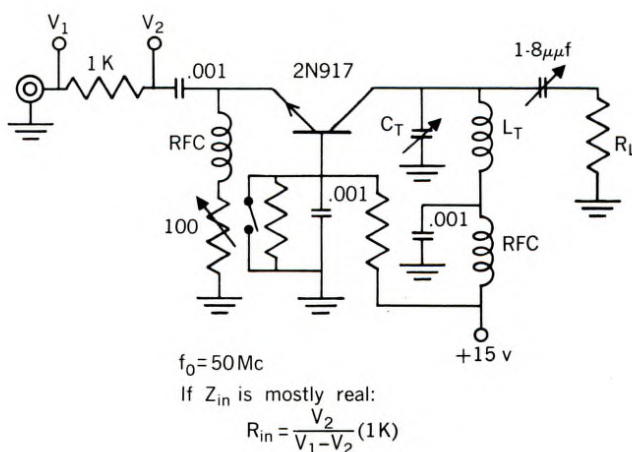


Figure 10—Buffer test circuit.

SAMPLE TRANSMITTER DESIGN

Proposed Requirements

As an example of VHF transistor transmitter design, take a requirement for a telemetry transmitter in an earth satellite where rugged environmental stresses are encountered and advanced performance is required. Such a unit must be small, light in weight, efficient, reliable, operate over a wide temperature range in a vacuum, be mechanically sturdy, and generally demonstrate performance that is consistent with the state of the art. The initial requirements are, then:

Efficiency, $> 25\%$

Weight, < 1 lb

Temperature, 0° to 100°C

Spurious emission, > 60 db below carrier

Output frequency, 136.500 Mc

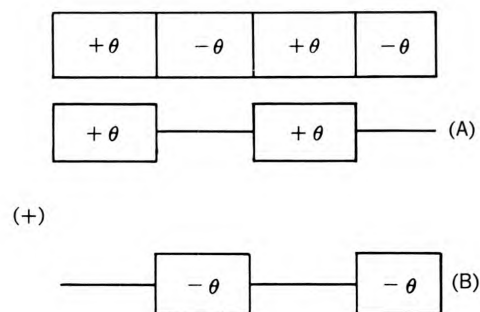
System Design

Modulation Method

The first part of the system to decide upon is the type of modulation to be used. Of the various methods in common use today, phase modulation (PM) was chosen for several practical reasons. First of all, PM is readily compatible with the synchronous detection systems presently in use by the NASA tracking stations. This linear detection process allows use of post-detection filtering to best advantage. Second, PM, by reason of its constant amplitude carrier wave, permits the transmitter RF circuits to be adjusted for maximum efficiency without regard to linearity. Third, with the constant amplitude square wave deriving from pulse-type encoding systems, the proportion of output power in the sidebands can be easily adjusted from 0 to 100 percent – depending on requirements – by setting the index of modulation.

For this transmitter, it was decided to make the power in the carrier equal to that in each of the principal sidebands. This condition provides a large proportion of power in the information sidebands, yet it leaves sufficient power in the carrier for tracking purposes. The proper modulation level can be adjusted quite easily by observing the spectrum on a panoramic display unit.

To find the required modulation index for square wave modulation, the constant amplitude, phase-switching carrier is broken into two amplitude-modulated components:



Each component is a constant phase, amplitude-modulated carrier that can easily be analyzed by Fourier series, and whose spectra can be added to obtain the spectrum of the original phase-modulated wave:

$$\begin{aligned}
 A &= \sin(\omega_c t + \theta) \left\{ \frac{k}{2} + \frac{2k}{\pi} \left[\cos \omega_m t + \frac{1}{3} \cos 3\omega_m t + \frac{1}{5} \dots \right] \right\} \\
 &= \frac{k}{2} \sin(\omega_c t + \theta) + \frac{k}{\pi} \left\{ \cos \left[(\omega_c - \omega_m) t + \theta \right] + \cos \left[(\omega_c + \omega_m) t + \theta \right] \right. \\
 &\quad \left. + \frac{1}{3} \cos 3 \left[(\omega_c - \omega_m) t + \theta \right] + \frac{1}{3} \cos 3 \left[(\omega_c + \omega_m) t + \theta \right] + \dots \right\} , \\
 B &= \frac{k}{2} \sin(\omega_c t - \theta) + \frac{k}{\pi} \left\{ \cos \left[(\omega_c - \omega_m) t - \theta \right] + \cos \left[(\omega_c + \omega_m) t - \theta \right] \right. \\
 &\quad \left. + \frac{1}{3} \cos 3 \left[(\omega_c + \omega_m) t - \theta \right] + \frac{1}{3} \cos 3 \left[(\omega_c - \omega_m) t - \theta \right] + \dots \right\} , \\
 A + B &= k \cos \theta \sin \omega_c t + \frac{2k}{\pi} \sin \theta \left\{ \sin(\omega_c - \omega_m) t \right. \\
 &\quad \left. + \sin(\omega_c + \omega_m) t + \frac{1}{3} \sin 3(\omega_c - \omega_m) t \right. \\
 &\quad \left. + \frac{1}{3} \sin 3(\omega_c + \omega_m) t + \dots \right\} .
 \end{aligned}$$

Setting the amplitude coefficients of the principal sidebands and the carrier equal,

$$\begin{aligned}
 k \cos \theta &= \frac{2k}{\pi} \sin \theta , \\
 \frac{\sin \theta}{\cos \theta} &= \tan \theta = \frac{\pi}{2} , \\
 \theta &= 57.5^\circ \approx 1 \text{ radian} .
 \end{aligned}$$

To find the proportion of power in the carrier and sidebands, the total radiated power is needed. This can be found by setting $\theta = 0$, whereupon all of the power is in the carrier:

$$\begin{aligned}
 P_{\text{total}} &= (k \cos 0)^2 = k^2 , \\
 \frac{P_c}{P_{\text{total}}} &= \frac{(k \cos \theta)^2}{k^2} = \cos^2 57.5 , \\
 P_c &= 29\% P_T ,
 \end{aligned}$$

$$\frac{P_1}{P_{\text{total}}} = 2 \frac{\left(\frac{2k}{\pi} \sin \theta\right)^2}{k^2} = \frac{8}{\pi^2} \sin^2 57.5^\circ,$$

$$P_1 = 58\% P_{\text{total}},$$

$$P_{>1} = P_{\text{total}} - P_c - P_1 = 13\% P_T.$$

Power Output

Because there are so many factors relating to total system performance that affect the calculation of the required power output of the transmitter, it is impossible to produce an exact number without knowing more about the particular application involved. The output of this sample design was therefore chosen arbitrarily as 1 watt. Figure 11 shows the available power at the receiver for a typical antenna system and a 1-watt transmitter at various ranges.

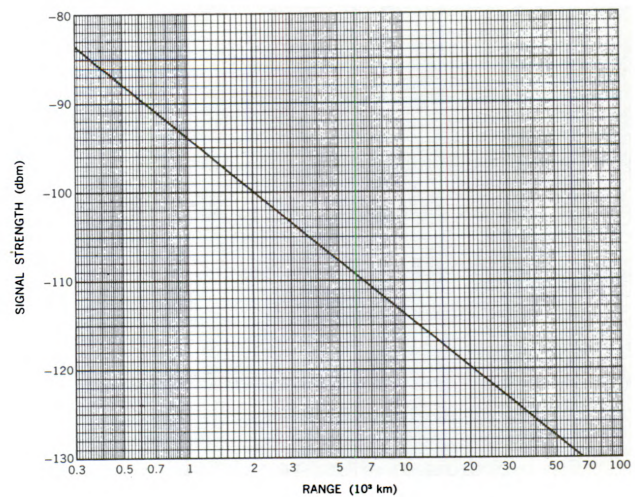
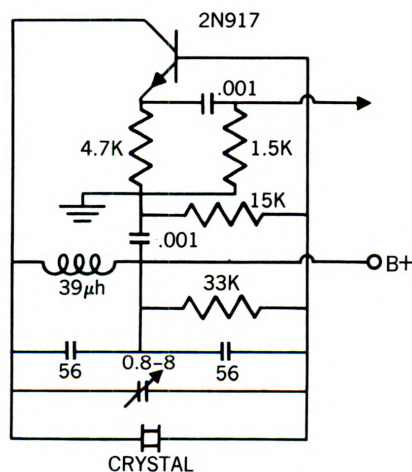


Figure 11—Signal strength vs. range. $P_T = 1$ watt; $G_T = -3$ db; $G_r = +20$ db; system loss = -6 db; $P_r = A_{\text{eff}} S$, with $S = P_T / 4\pi r^2$ and $A = G_r \lambda^2 / 4\pi$.

Circuit Details

Oscillator



In an earth-satellite telemetry application, the Doppler shift due to the satellite velocity will have a large effect on the apparent transmitter frequency as seen from the ground. There is, then, little to be gained by requiring a long-term frequency stability and calibration of the transmitter oscillator to much closer limits than the Doppler shift itself. If the frequency tolerance is set equal to this

velocity shift for an "average" orbit,

$$\text{Tolerance} = \frac{\Delta f}{f_0} = \frac{v \cos \phi}{c} \approx \pm 0.002\%$$

where

ϕ = the angle between the observer and the velocity vector,

v = velocity of satellite,

c = velocity of light.

A frequency tolerance of ± 0.002 percent can be obtained with commercially available quartz crystals without using temperature-controlled ovens or frequency compensation techniques.

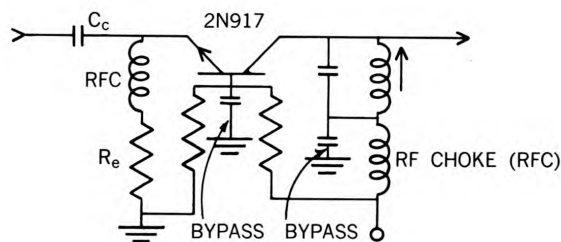
High orders of short-term stability are required, however, because of the phase-lock detection system commonly in use for satellite tracking and telemetry reception. Steps should be taken, therefore, to prevent frequency shifts due to modulation or supply voltage transients.

To meet these requirements, a modified Pierce oscillator [Figure 4(c)] was chosen. As is shown in Figures 3 and 5, this circuit provides good isolation of the oscillator frequency from circuit elements and loading effects. The output impedance is very low because of the negative feedback in the emitter. This low output impedance provides the good load isolation. The absence of any tuned elements in the circuit other than the crystal enhances the crystal's control over the frequency of oscillation, which improves the stability.

The Pierce oscillator is essentially a crystal-controlled Colpitts circuit. The crystal oscillates in an anti-resonant mode, and feedback is controlled by the ratio of the two series capacitors across the crystal and the emitter load resistance. The series equivalent of these two capacitors, added to that of the variable trimmer, determines the crystal load capacity, which is usually set to $32 \mu\mu\text{f}$. The variable trimmer allows close calibration of the oscillator frequency by "pulling" the crystal. A 2N917 transistor is used because it has a maximum frequency of oscillation of 1000 Mc. This high cutoff frequency means that the inherent phase shift in the device at low frequencies is negligible and better stability will result.

Because the oscillator has no tuned circuits, oscillation can occur only on the fundamental mode of the quartz crystal. This limitation sets an upper limit on the oscillator frequency of 20 Mc, since this is the highest frequency fundamental crystal that can be obtained. The lowest order, non-prime submultiple of the output frequency of 136.5 Mc is 17.0625 Mc. Therefore, a frequency multiplication of 8 is required between the oscillator and the transmitter output.

Buffer Amplifier



The output from the oscillator was experimentally measured at about 1 mw. Since this output is insufficient to drive a class B or C amplifier stage, the buffer amplifier must be operated class AB. A 2N917 transistor is used because of its high gain, high frequency rating, and efficiency. The design procedure follows:

$$V_{cc} = \frac{1}{2} V_{cb} = + 15 \text{ volts} .$$

Very little information on large signal operation is given by the manufacturer. The only known quantities are:

$$P_{in} = 1 \text{ mw} ,$$

$$R_{in} \approx \frac{1}{\text{Re } Y_{ib}} = 300 \text{ ohm}$$

and the relations

$$P = \frac{V_c^2}{2R_L} = \frac{(V_{cc} - V_{min})^2}{2R_L} ,$$

$$G_P \approx \frac{R_L}{R_{in}} ,$$

which, when combined, yield

$$P_o^2 = \frac{V_c^2 P_{in}}{2R_{in}} .$$

For this circuit,

$$P_o = 14 \sqrt{\frac{10^{-3}}{600}} = 18 \text{ mw} ,$$

$$R_L = \frac{V_c^2}{2P_o} = \frac{(14)^2}{2(18)} = 5.5 \text{ K} ,$$

$$X_T = \frac{R_L}{Q} = \frac{5.5 \text{ K}}{10} = 550 \text{ ohm} ,$$

$$f_0 = 17.0625 \text{ Mc} ,$$

$$C_T = 17 \mu\mu\text{f} \text{ (this includes collector capacity and that reflected from the coupling network),}$$

$$L_T = 5 \mu\text{h} .$$

Assuming $Q_T \approx 100$,

$$\eta_T = 1 - \frac{Q_{loaded}}{Q_T} = 0.9 ,$$

$$P_o' = 0.9 (18) = 16 \text{ mw} ,$$

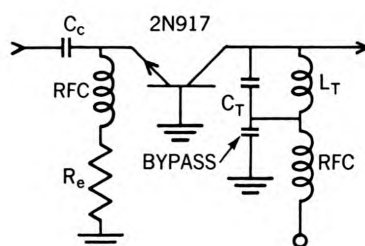
For a rough approximation of the dc power required, assume the collector efficiency is typically 50 percent.

$$P_{dc} = \frac{P_o'}{0.5} = 32 \text{ mw} ,$$

$$I_{dc} = \frac{P_{dc}}{V_{cc}} = \frac{32}{15} = 2.1 \text{ ma} .$$

The bias network is adjusted to produce a collector current of about 0.5 ma under no-signal conditions.

First Frequency Multiplier



The required 8-times-frequency multiplication is most easily achieved with three cascaded frequency doublers. The first frequency multiplier doubles the 17.0625 Mc output from the buffer amplifier to 34.125 Mc. A 2N917 transistor is used.

$$R_{in} = \frac{1}{Re Y_{ib}} = 300 \text{ ohms} ,$$

$$X_c = \sqrt{R_L R_{in}} = 1.3 \text{ K} ;$$

therefore,

$$C_c = 7.2 \mu\text{f} .$$

If the amplifier were a straight-through class B stage,

$$P_{o,1} = V_c \sqrt{\frac{P_{in}}{2R_{in}}} = 14 \sqrt{\frac{16}{2(0.3)}} = 72 \text{ mw} .$$

But, since the stage is operated class C over a short conduction angle, the gain will be about 2 db smaller (see Figure 7). An exact figure for the increased drive requirement can be obtained only by Fourier analysis of the input waveform, which cannot be done under the circumstances. Experience provides the only answer.

$$P'_{o,1} = P_{o,1} - 2 \text{ db} \approx 50 \text{ mw} ,$$

$$I_{c,1} = \sqrt{2} \frac{P'_{o,1}}{V_c} = 5.1 \text{ ma, rms} .$$

For a frequency doubler, the conduction angle should be about 110 degrees (Reference 1). Fourier analysis shows the ratio of fundamental current in the collector pulses (assuming a square law device) to be (Reference 1):

$$I_{c,2} = \frac{0.25}{0.30} I_{c,1} = 4.25 \text{ ma} ,$$

$$P_{o,2} = \frac{V_c}{\sqrt{2}} I_{c,2} = 42 \text{ mw} .$$

Assuming

$$\eta_T = 0.9 ,$$

then

$$P'_{o,2} = 38 \text{ mw} .$$

For better temperature stability it is desirable to run the doubler in a saturated condition. To accomplish this state, about 1 db of gain is wasted and the output is designed for 30 mw.

$$R_L = \frac{V_c^2}{2P_o} = 3.3K ,$$

$$X_T = \frac{R_L}{Q} = 330 \text{ ohms} ,$$

$$f_o = 34.125 \text{ Mc} ,$$

$$L_T = 1.5 \mu h ,$$

$$C_T = 14 \mu\mu f \text{ (including collector and reflected capacity).}$$

To obtain the required conduction angle of 110 degrees,

$$\left(V_{in-peak} \right) \left(\cos \frac{\theta}{2} \right) = V_{bias} + V_{diode} ,$$

$$V_{in} = \sqrt{2} \sqrt{P_{in} R_{in}} = 3.2 \text{ volts} ;$$

so

$$V_{bias} = 3.2 \cos (55^\circ) - 0.7 = 1.1 \text{ volts} .$$

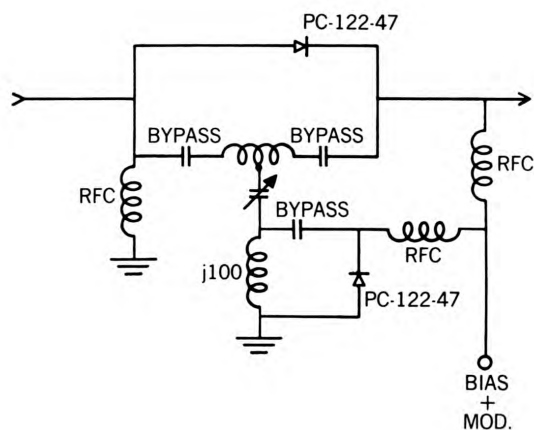
Experiment indicates that a typical collector efficiency for a doubler stage is about 40 percent.

$$P_{dc} = \frac{P_{0,2}}{\eta_c} = \frac{30}{0.4} = 75 \text{ mw} ,$$

$$I_{dc} = \frac{P_{dc}}{V_{cc}} = 5 \text{ ma} ,$$

$$R_e = \frac{V_{bias}}{I_{dc}} = \frac{1.1}{5} = 220 \text{ ohms} .$$

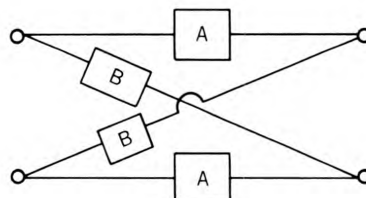
Modulator



The phase modulator uses voltage-variable capacitors in a transformation of a lattice all-pass network (Reference 2). The circuit development follows the following steps:

$$A = jX ,$$

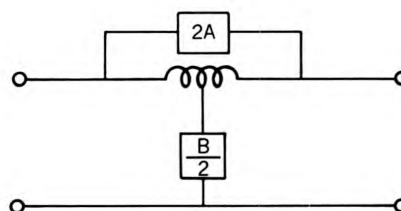
$$B = \frac{Z_0^2}{A} ,$$



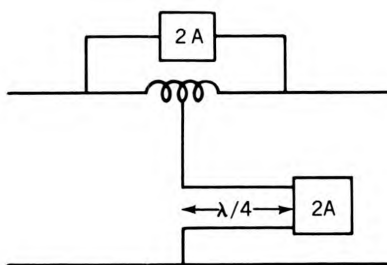
which can be transformed to

$$\alpha = 0 ,$$

$$\beta = 2 \tan^{-1} \left(\frac{X}{Z_0} \right) .$$



To make a phase modulator of this network, the phase must be varied electronically. This can be done by making A and B electronically variable; but A and B are opposite reactances, between which a reciprocal relation must be maintained. These conditions can be met, however, if a quarter-wave transmission line of impedance Z_0 is inserted in B:



If A is a variable capacitance diode, the phase can be made electronically variable. By shunting the diode with some fixed inductance, the nonlinear C versus V function can be made to compensate for the tangent phase-function nonlinearities. Linearity can be maintained for a modulation index of well over 1 radian. In a practical circuit, the quarter-wave transmission line is made from lumped elements, and the transformer provides the shunt inductance.

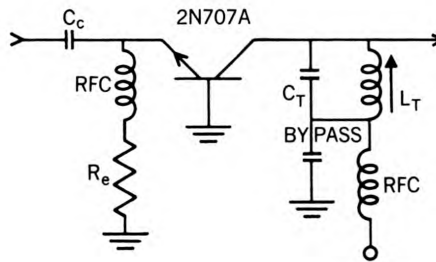
Since the reverse bias voltage on the diodes is only a few volts, the power handling capacity of the modulator is small if the diodes are not to conduct. The maximum RF signal power is:

$$P = \frac{V_d^2}{2R_0} \text{ watts} .$$

Obviously, if the device is to handle even a few tens of milliwatts, its characteristic impedance must be low. A practical Z_0 is on the order of 100 ohms.

For the reason just stated and because the frequency multipliers will also multiply the modulation index (thus requiring less from the modulator), it is desirable to place the modulator as near the oscillator as practical. On the other hand, modulating too close to the oscillator will cause incidental FM from lack of isolation. In this transmitter it is placed between the first and second frequency doublers. Thus, the oscillator is protected by the buffer and first doubler. Yet the power level is still only 30 mw, and the second and third doubler will multiply the modulation index by a factor of 4. For an output index of 1 radian, only 0.25 radian is required from the modulator. Since $Z_0 = 100$ ohms and $V_{bias} = -4$ volts, then $P_{max} = 80$ mw and $C_c = 8.5 \mu\mu f$. Because the loss = 2 db, then $P_{out} = 19$ mw.

Second Frequency Multiplier (Doubler)



Looking ahead to the requirement of a higher voltage supply for the final amplifier, it would be wise to use higher voltage transistors for all of the remaining stages. If this is done, only one supply voltage would be required for the transmitter since the three low level stages already designed could be zener-regulated at the lower voltage with only a small loss in efficiency. A regulated voltage for the oscillator and buffer would be desirable for stability anyway. A convenient value for the supply voltage might be + 24 volts, since this seems to be almost a standard voltage in many electronic systems – particularly in military systems.

With this requirement in mind, a 2N707 transistor is a good choice. The field of possible transistors to choose from is restricted, by the upper temperature limit, to silicon devices, which have not quite caught up with the state of the art in germanium transistors. Unfortunately, very little information is available from the manufacturer about the 2N707 transistor; they state only that at 100 Mc it will develop 300 mw output with 7.5 db gain. With such inadequate data, the most reliable (and fastest) procedure is to breadboard the amplifier and determine the results experimentally. For a very rough approximation, R_{in} can be calculated from the data given and the assumption made that it is independent of frequency (which it is not).

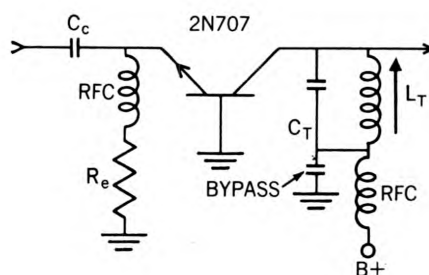
$$R_{in} = \frac{R_L}{G_p} = \frac{V_c^2}{2P_o G_p} = \frac{(19)^2}{2(300)(6)} = 100 \text{ ohms}$$

This impedance, conveniently, is just the right value for the modulator load, and no matching is required. Through a process like that used for the design of the first doubler, and allowing 2 db surplus gain for temperature and voltage variations, a rough design can be made for the second doubler:

$$\begin{aligned}
 P_{o,2} &= 60 \text{ mw} , \\
 R_L &= 4.4 \text{ k} \\
 C_T &= 10.5 \mu\mu\text{f} \\
 L_T &= 0.5 \mu\text{h}
 \end{aligned}
 \left. \vphantom{\begin{aligned} P_{o,2} \\ R_L \\ C_T \\ L_T \end{aligned}} \right\} Q = 20$$

$$\begin{aligned}
 I_{dc} &= 6 \text{ ma} , \\
 R_e &= 47 \text{ ohms} .
 \end{aligned}$$

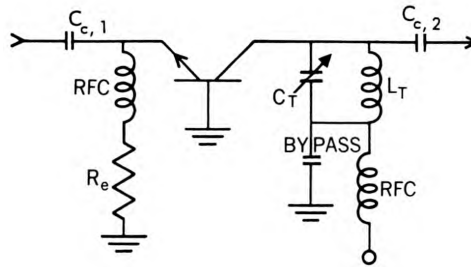
Third Frequency Multiplier (Doubler)



Design of the third doubler proceeds exactly like that of the second doubler:

$$\begin{aligned}
 R_{in} &\approx 100 \text{ ohms} , \\
 C_c &= 3.6 \mu\mu\text{f} , \\
 P_{o,2} &= 110 \text{ mw} , \\
 R_L &= 2.4 \text{ K} , \\
 C_T &= 10 \mu\mu\text{f} , \\
 L_T &= 0.15 \mu\text{h} , \\
 I_{dc} &= 11 \text{ ma} , \\
 R_e &= 90 \text{ ohms} .
 \end{aligned}$$

Final Amplifier



At this point in the design, we will jump to the final amplifier and work backward, the reason being that this stage must be designed for a specific predetermined output power. The parameters of the other stages must be adjusted to meet the requirements of this final amplifier. An RCA TA2267 transistor was selected for the circuit. This transistor has a collector breakdown voltage of 60 volts and would therefore work best with $V_{cc} = 30$ volts. Performance should be satisfactory at 24 volts, however.

Conveniently, the manufacturer provides measured curves showing the gain of the device versus frequency and output power. With a power output of 1 watt and a frequency of 136 Mc, these curves show a typical drive requirement of 250 mw for class C operation. While the curves are measured for a common emitter configuration, the power gain should not be radically different for grounded base operation at this frequency. So, for this circuit,

$$R_L = \frac{(V_{cc} - V_{min})^2}{2P_o} = \frac{23^2}{2(1)} = 265 \text{ ohms} ,$$

$$X_T = \frac{R_L}{Q} = 26.5 \text{ ohms} ,$$

$$C_T = 44 \mu\mu f ,$$

$$L_T = 0.03 \mu h ,$$

$$X_{c,2} = \sqrt{R_L R_{out}} = \sqrt{265(50)} = 115 \text{ ohms} ,$$

$$C_{c,2} = 10 \mu\mu f .$$

Since G_p - as read from the curves - is for "class C" operation, the "class B" G_p is probably about 6.5 instead of 4. So,

$$R_{in} = \frac{R_L}{G_p} = 40 \text{ ohms} ,$$

$$X_{c,1} = \sqrt{R_{L-driver} R_{in}} = \sqrt{\frac{V_c^2}{2P_{in}} R_{in}} = 200 \text{ ohms} ,$$

$$C_{c,1} = 6 \mu\mu f .$$

Choosing

$$\theta = 140^\circ \text{ (see Reference 1),}$$

$$V_{in} = \sqrt{R_{in} P_{in}} = 3.1 \text{ volts} ,$$

$$V_{bias} = \sqrt{2} V_{in} \cos\left(\frac{\theta}{2}\right) - 0.7 = 0.8 \text{ volt} .$$

Assuming

$$\eta_c \approx 0.5 ,$$

then

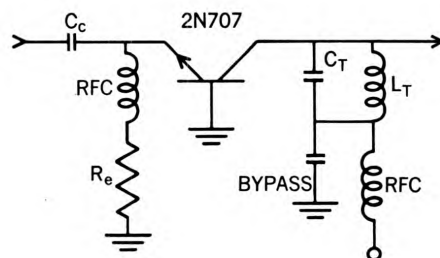
$$P_{dc} \approx \frac{P}{\eta_c} = 2 \text{ watts} ,$$

$$I_{dc} = \frac{P_{dc}}{V_{cc}} = \frac{2}{24} = 83 \text{ ma} ,$$

$$R_e = \frac{V_{bias}}{I_{dc}} = \frac{0.8}{0.083} = 10 \text{ ohms} .$$

Since the RF choke required in series with R_e has a resistance of 2 ohms, the actual R_e required is approximately 8 ohms.

Driver



Observing that the final amplifier requires 250 mw driving power and that the third doubler only puts out about 100 mw, it becomes obvious that an extra stage of amplification is required. Since another amplifier will certainly provide more than the 4 db of gain required, a considerable surplus of gain will be available. Because of the loss of efficiency it is not advisable to overdrive the final power amplifier, so the excess power gain must be taken up in lower power stages where the cost in efficiency will not be so high. Accordingly, the driver stage is designed for a power output of 250 mw:

$$P_o = 250 \text{ mw},$$

$$f_o = 136.5 \text{ Mc},$$

$$\eta_T = 0.9 \text{ (assumed),}$$

$$R_{in} = 100 \text{ ohms (approx.),}$$

$$P_o' = 280 \text{ mw},$$

$$G_P \approx \frac{R_L}{R_{in}} \approx 10 \text{ db (class B),}$$

$$R_L = 950 \text{ ohms},$$

$$P_{dc} \approx \frac{P_o}{0.5} \approx 500 \text{ mw},$$

$$C_T = 12 \mu\mu\text{f},$$

$$I_{dc} \approx \frac{P_{dc}}{V_{cc}} = \frac{500}{24} = 21 \text{ ma.}$$

$$L_T = 0.1 \mu\text{h},$$

Since so much surplus gain is available, the driver can be operated with a very short conduction angle to trade some of its extra gain for better efficiency. Let

$$\theta = 100^\circ,$$

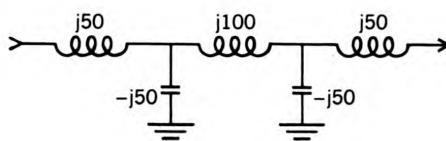
$$V_{in} = \sqrt{2P_{in} R_{in}} = \sqrt{20} = 4.5 \text{ volts peak},$$

$$V_{bias} = 4.5 \cos(50^\circ) - 0.7 = 2.2 \text{ volts},$$

$$R_e = \frac{V_{bias}}{I_{dc}} = \frac{2.2}{0.021} = 100 \text{ ohms}.$$

The rest of the extra gain should be used in the frequency multiplier stages in a similar fashion by increasing the bias on these stages and therefore decreasing their conduction angle.

Harmonic Suppressor



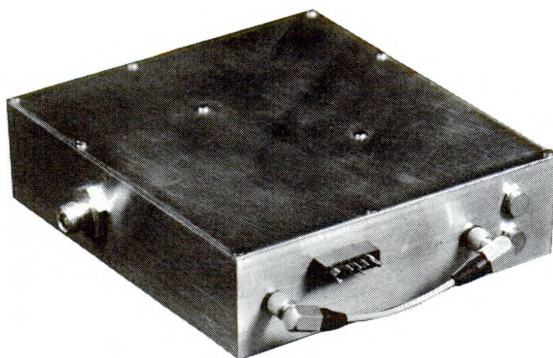
Since transistors are inherently such good harmonic generators, some means must be provided to attenuate this spurious radiation to prevent interference with other services. Good harmonic suppression can be achieved simply by insertion of an artificial half-wave transmission line in the transmitter output. At the output frequency, the antenna load is transmitted faithfully through to the transmitter and the output energy is delivered to the antenna with negligible loss. At the harmonic frequencies, however, the artificial line is no longer matched nor is it still one-half wave long. The harmonic energy is attenuated by the mismatch thus produced. At the same time, the impedance of the shunt capacitors in the line is decreased and the impedance of the series inductors is increased by the higher frequency of the harmonics. This action tends to bypass what harmonic energy is in the line to ground. Actual measured values for one of these artificial lines are:

Harmonic (N)	Freq. (Mc)	Loss (db)
1	136.5	0.2
2	273	33
3	410	53
4	548	62
5	685	56
6	820	58
7	955	61

The flattening of the attenuation curve at the fourth harmonic is due to series resonance of the standoff-type shunt capacitors with their lead inductance and capacitive coupling around the series inductors. An identical unit built with shielded sections and feed-through capacitors measured 84 db rejection at 955 Mc, and was still increasing. But, since harmonics of such high orders should be negligible in the transmitter output, the extra attenuation provided is probably not worth the increased complexity of construction.

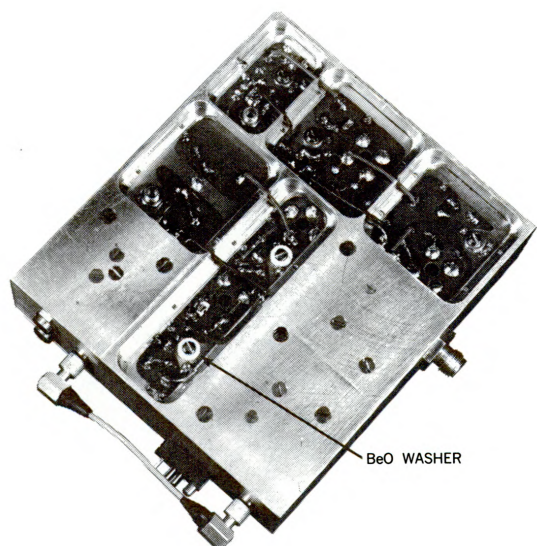
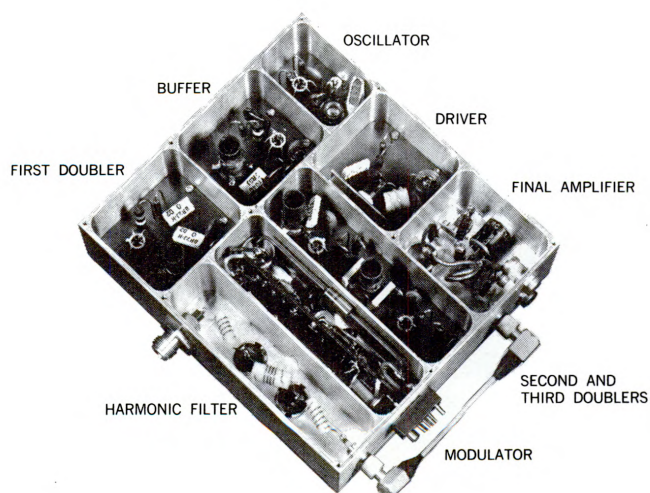
Mechanical Considerations

To provide good shielding, a compartmented chassis milled from an aluminum block is used, as shown in Figures 12(b) and (c). The compartment walls, in addition to shielding the various stages, also stiffen up the whole chassis against mechanical vibration. Printed circuit construction is used where feasible to increase ease of fabrication and uniformity of performance. For better resistance to mechanical stress and vibration, the whole chassis can be filled with a low dielectric encapsulating material, such as Eccofoam FP. Repairs or modifications of a completed unit can then most easily be made by replacement of whole modules, although the potting material can be removed by careful picking with a small knife or scribe.



a. Oblique view

b. Top view



c. Bottom view

Figure 12—Transmitter.

Thermal Problems

Since equipment in a satellite or space vehicle must operate in a vacuum, special attention must be paid to the problem of removing the heat dissipated by the transistors. With no air to circulate, heat can be removed only by radiation or direct conduction; but, since

$$P_{\text{rad}} \sim \Delta T^4,$$

the radiation mechanism is efficient only at elevated temperature gradients. The only practical method for heat transfer in the unit is therefore direct conduction. A thermal path must be provided from each transistor case to the aluminum chassis, which should be fastened directly to the spacecraft structure. Thermal paths can be supplied on the printed circuit boards by the copper lamination, to which the transistor case can be fastened through a clamp of some fashion. If the transistor case is common to one of the leads, electrical isolation must be provided by the heat sink without degrading the thermal path too much. An excellent material for use in such a situation is beryllium oxide, which has a coefficient of thermal conductivity about equal to that of aluminum and yet demonstrates a high resistivity and low dielectric loss. Much use has been made in the past of thin slices of mica, Teflon, or Mylar for electrically insulated heat sinks. Although the thermal conductivity of these materials is poor, the fact that they are cut very thin limits the extent of the thermal path through them and therefore the temperature gradient. The very low thickness of the material causes a large capacity from the transistor case to ground, however, which limits their application in VHF circuits.

In this transmitter, the transistors are mounted in a clamp of the type shown in Figure 13. The clamp is then bolted to the copper lamination of the printed circuit board with a BeO washer as a spacer. The clamp is mounted as near to the chassis as feasible to keep the thermal path short (see Figure 14). Assuming that the thickness of the copper is 2/1000 inch and the thermal path length in the copper is 1/4 inch, the "thermal resistance" is

$$\mathcal{R} = \frac{\Delta T}{P} = \frac{l}{kA},$$

where

l = path length in cm,

A = area in cm^2 = wt,

k = coefficient of conduction,

$$\mathcal{R} = \frac{0.25 (2.54)}{2 (2 \times 10^{-3}) (0.25) (2.54)^2} \approx 100^\circ\text{C/watt}.$$

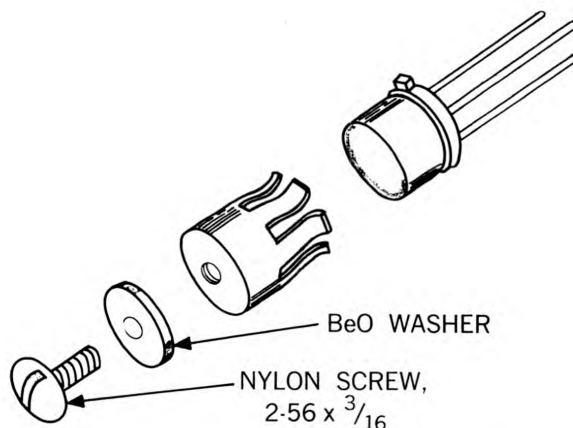
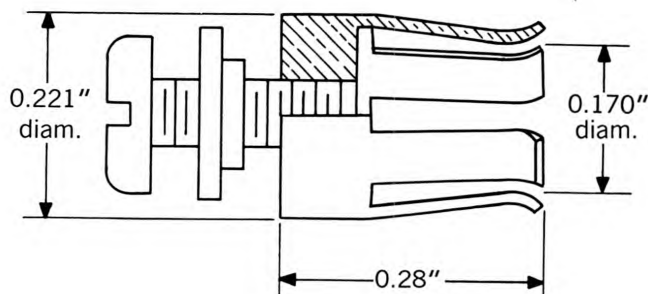


Figure 13—Heat dissipator and retainer for TO-18 transistors.

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Obviously, this method of heat sink is adequate only for stages dissipating 100 mw or less. The temperature gradient across the other components of the heat path can be neglected, compared with this relatively high value. To provide the required heat capacity, the higher powered stages are clamped directly to the chassis. This technique complicates the construction procedure somewhat but is necessary to keep the transistors adequately cooled. Where large amounts of heat are dissipated, even the areas of contact between the heat-sink components can become critical heat problems. In a vacuum, with no air to fill the microscopic voids in the contact surfaces, the actual area of conduction may be only 1 percent of the geometrical area. To reduce this problem, all areas of contact in a heat sink for a high power transistor should be cemented.

As an example of the thermal design of a transistor amplifier, we will examine the third doubler stage:

$$\mathcal{R}_{\text{transistor}} = 150^{\circ}\text{C}/\text{watt} ,$$

$$\mathcal{R}_{\text{heat sink}} = 100 ,$$

$$\mathcal{R}_{\text{total}} = 250 ,$$

$$P_{\text{dissipated}} = P_{\text{dc}} - P_o = 260 - 110 = 150 \text{ mw} ,$$

$$\Delta t = \mathcal{R}P = 250(0.15) = 37.5^{\circ}\text{C} ,$$

$$T_j (\text{max. junction temp.}) = 175^{\circ}\text{C} ;$$

therefore,

$$T_{\text{chassis max.}} = T_j - \Delta T = 137.5^{\circ}\text{C} .$$

A reliable design always will include safety factors so that degradation of components, accidental operation just outside of the specified temperature range, and unforeseen operating conditions might not cause failure of the transmitter. The final amplifier should always be designed so that it can dissipate the full dc input power as heat, in case the unit is operated without the antenna connected or under conditions of high standing wave ratio.

The calculated maximum chassis temperatures, in degrees Centigrade, for the other stages in the transmitter are:

Oscillator — 180°

Buffer — 190°

First doubler — 177°

Second doubler — 155°

Driver — 135°

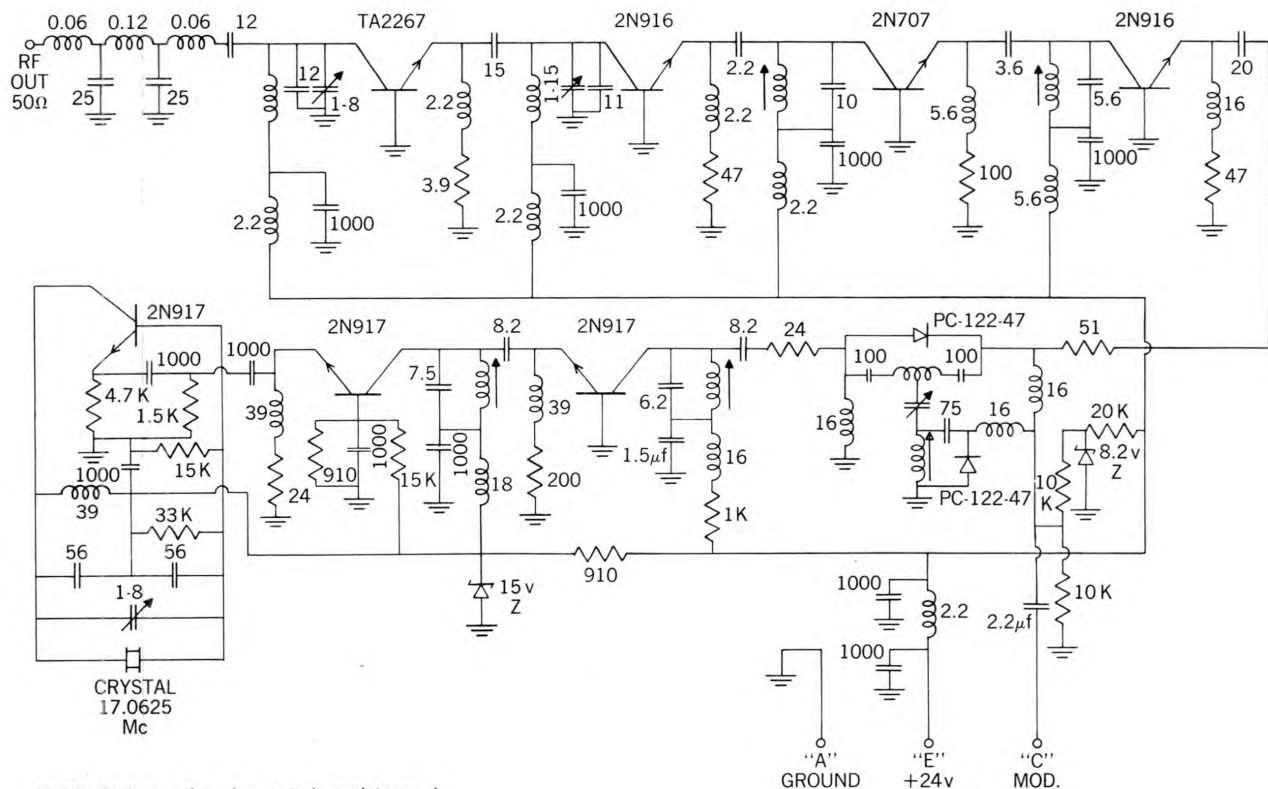
Final amplifier — 140°

Experimental Verification

As a verification of the sample design presented previously, the transmitter was constructed as seen in Figure 12. The unit performed as predicted with two notable exceptions. In spite of precautions, a regenerative feedback problem developed in the driver stage. This problem was eliminated by replacing the 2N707 transistor with a 2N916, which apparently has less internal feedback. Otherwise, the two transistors have similar ratings.

The second unforeseen complication was an interaction of the modulator on the buffer stage tuning. Some resistive padding was required to better match the modulator input and output so as to minimize this effect. The additional loss of the padding necessitated replacing the 2N707 in the second doubler stage with a 2N916, which has just enough extra gain to compensate.

The final schematic diagram is shown in Figure 14. Some minor variations from the design can be found where adjustments were necessary to obtain proper performance. For example, the input impedance of the final amplifier turned out to be somewhat lower than what was calculated. This necessitated increasing the interstage coupling capacitor and lowering the bias resistor. The resultant performance parameters are given in Table 1 and Figure 15. Performance at -10°C and below deteriorates fairly rapidly. This could be extended to lower values, at a slight cost in efficiency, by the use of diode compensation in the low level stages.



NOTE: Unless otherwise noted, resistance is in ohms, capacity in μmf , inductance in μH

Figure 14—The transmitter.

Table 1
Transmitter Performance .*

T(°C)	P ₀ (dbw)	I (ma)	Δf_0 (cps)	FM (cps)	AM (%)
0	-0.7	140	+450	0	5
10	-0.6	142	+403	1	3
25	-0.5	148	-78	1	0
40	-0.4	150	-200	2	0
60	-0.2	155	-350	1	4
80	-0.2	152	-174	2	4
100	-0.3	148	+840	2	2

* $f_0 = 136.500$ Mc
 $\eta = 28\%$

$\theta_p = 1$ radian
 $V = +24$ volts $\pm 10\%$

Weight = 247 gm, unpotted
Estimated weight potted <300 gm,

2nd harmonic = 55 db below carrier
3rd harmonic = 80 db below carrier

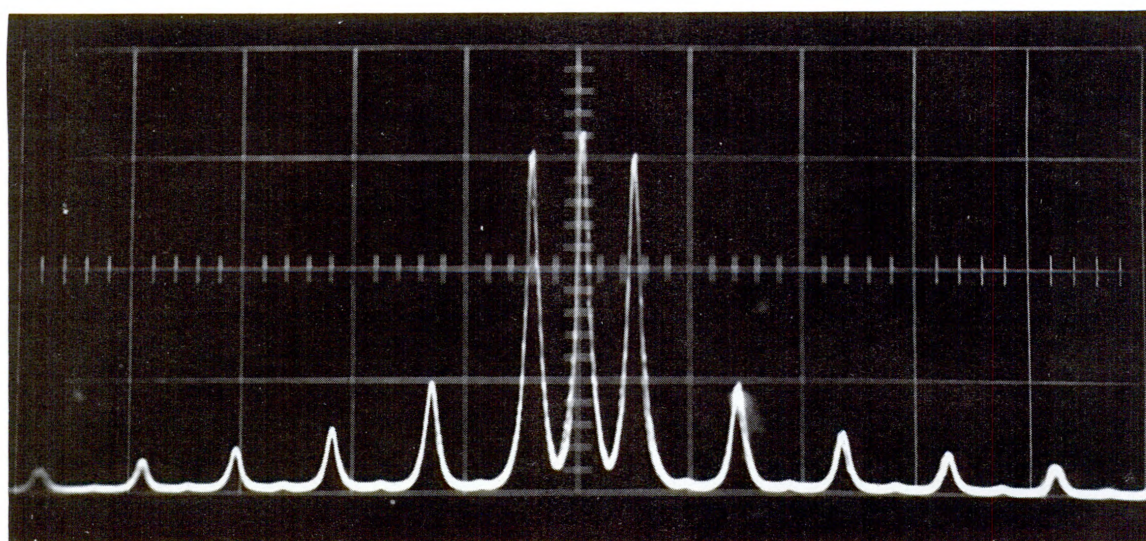


Figure 15—Spectrum for square wave modulation.

(Manuscript Received June 21, 1963)

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Appendix A

List of Symbols

A_{eff}	effective capture area of antenna
C	capacity
C_c	interstage coupling capacity
C_T	tank circuit capacity
c	velocity of light
f	frequency
f_0	nominal frequency
G_i	current gain
G_P	power gain
G_r	receiving antenna gain
G_T	transmitting antenna gain
$I_{c,1}$	fundamental frequency collector current
$I_{c,2}$	2nd harmonic collector current
I_{dc}	direct current collector current
I_{in}	input signal current
I_{out}	output signal current
jX	reactance
k	constant of proportionality
L_T	tank circuit inductance
l	path length (cm)
P	power
P_c	power in carrier only
P_{dc}	direct current power
P_{in}	driving power
P_o	output power
$P_{o,1}$	fundamental frequency output power

$P_{o,2}$	2nd harmonic output power
P_r	received power
P_{rad}	radiated power
P_T	transmitted power
P_{total}	power in carrier and sidebands combined
P_1	power in principal sideband
$P_{>1}$	power in sidebands of order greater than 1
Q	quality factor
Q_{loaded}	loaded Q of a tank circuit
Q_T	unloaded Q of a tank circuit
\mathcal{R}	thermal resistance
R_e	emitter bias resistor
R_{in}	input signal resistance
R_L	collector load resistance
R_{out}	output signal resistance
R_0	real part of Z_0
S	flux density
T	temperature
$T_{chassis}$	ambient chassis temperature
T_J	maximum allowable transistor junction temperature
t	thickness
V_{bias}	required bias voltage
V_c	peak collector signal voltage
V_{cb}	maximum collector-to-base voltage
V_{cc}	collector supply voltage
V_{ce}	maximum collector-to-emitter voltage
V_d	diode reverse bias voltage
V_{diode}	forward bias necessary to cause current to flow
V_{min}	minimum collector voltage
V_{peak}	peak voltage
W	width
X_C	reactance of capacitor in tank circuit
X_c	reactance of coupling capacitor

X_L	reactance of inductor in tank circuit
X_T	reactance of tank circuit elements
Y_{ib}	common base input admittance
Z_0	characteristic impedance
α	attenuation
β	phase shift
η_c	collector efficiency
η_T	tank circuit efficiency
θ	modulation index of phase modulation (pages 9-11, 28); conduction angle (pages 16, 21-22)
λ	wavelength
ν	velocity of satellite
π	3.1416, approximately
ϕ	angle between observer and satellite
ω_c	angular carrier frequency
ω_m	angular modulation frequency